EE 505
Midterm Exam
Spring 2025

Due Tuesday April 1. Please place a hard copy under the office door of the instructor and upload an electronic version in Canvas. Problems on this exam should not be discussed with anyone other than the instructor of the class and, as such, all solutions should reflect individual efforts.

Problem 1

Consider an application where it is necessary to quantize a very slowly varying input that varies between 0V and 1V with a maximum error of 1 part in 8192.

a) If an ideal ADC is used (and no device noise is present), what is the minimum number of bits of resolution needed to meet these specifications?

b) What would be the INL specification required of an actual ADC with the same number of bits of resolution determined in part a) to meet the specified accuracy? How practical is it to achieve an ADC with his INL specification?

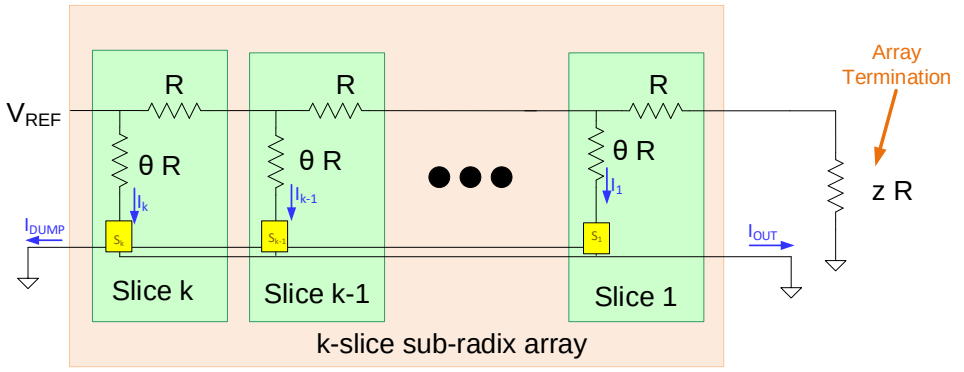
c) Give a practical strategy for setting specifications that can be realistically met.

Problem 2

A sub-radix ladder DAC is shown below where the parameter $\theta > 2$ and where the yellow blocks represents switch blocks that steer the current either to dump or to the output. For pure sub-radix operation, the termination resistor (designated as zR) must be selected so the impedance looking to the right into all slices (Slice k through Slice 1) is the same.

a) Derive the relationship between z and θ for proper termination (the expression for the relationship was given in course notes).

b) Determine the impedance facing V_{REF} in terms of R, z, θ, k.



Problem 3

The number of output levels in a DAC or the number of transition points in an ADC is typically an integer power of 2 and the number of bits of resolution is often stated as $\log_2 N$ where N is the number of levels in the data converter. Thus, the number of bits of resolution of a data converter is typically an integer. System designers are invariably aware of this and typically express a data converter requirement as an integer number of bits of resolution as well. Unfortunately the area of matching critical components in a data converter typically goes up by a factor of 4 for each additional bit of resolution for a given performance level and yield level. Thus, if the real system performance requirements are slightly more than that of a data converter with a resolution of an integer n_1, the system requirements would likely be specified to be that of an n_1+1 bit data converter. If we make the over-simplifying assumption that the cost of manufacturing a data converter is based only upon the matching critical area, it could be argued that the cost of an n_1+1 bit data converter would be almost a factor of 4 higher than the cost that is really required for the system if that performance is slightly above n_1 bits. Though most data converters have resolution characterized by an integer, it is not difficult to design a data converter that has a fractional number of bits of resolution. Consider now a system that requires a data converter with 150 output levels with outputs that must have $|INL_{kmax}|$ less than ¾ of a level (e.g. it could be a DAC with outputs between 0 and 1.2 volts that must have each output accurate to within ±6 mV) Assuming the cost of a data converter is only based upon the matching critical area, compare the cost of a data converter designed under the following 2 scenarios:

1. A 150-level DAC with V_{REF}=1.2V with an INL_{kmax} of .75 LSB was used
2. An 8-bit DAC with V_{REF}=1.2V with an I_{NLkmax} of 0.75 LSB was used

For convenience, you may assume that in both cases the DAC is a string DAC. When making this cost comparison, keep in mind that the cost must be based upon the cost/good DAC since DACs that do not meet the performance requirements will be assumed to be defective and thus destroyed.

Problem 4

It is well-known that the quantization noise decreases with the number of bits of resolution. Assume you are an engineering design manager and an aspiring engineer comes to you with a proposal for reducing the quantization noise of an R-string DAC without requiring any increase in area. The proposal goes like this. Assume a 10-bit string DAC has been designed with an area A allocated to the matching critical components at a given INL level. The aspiring engineer suggests increasing the number of bits of resolution to 12 bits to reduce the quantization noise while using the same total area in the matching-critical components. The argument is made that the absolute INL will not change since the same area is being used but the quantitation noise will be reduced to that of a 12-bit DAC. Comment on the validity of or the flaws in the argument.

Problem 5

Assume the only errors in a resistor string DAC are due to the random variation of the sheet resistance of the film and the only performance specification that must be met for a customer is the INL_{kmax}. For a particular 12-bit part, the customer will accept the part only if the INL_{kmax} is less than 1LSB.

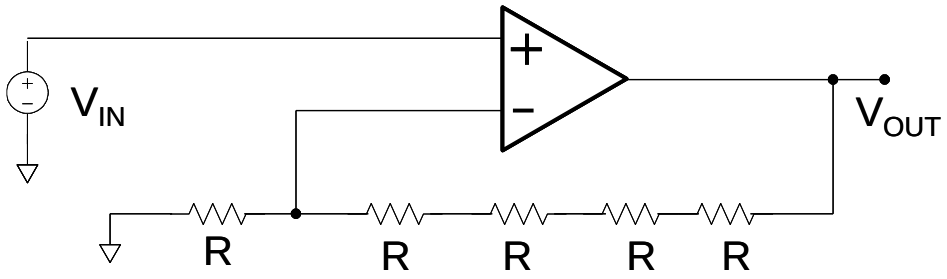
a) If the resistors in the DAC are square with a total active area of 102400μ^2, determine the yield of the 12-bit DAC if the process parameters for the sheet resistance are $A_\rho = 5\Omega \bullet \mu$ and $\rho_{NOM} = 30\Omega / sq$.

b) What will be the total resistance of the R-string?

c) How will the yield change if the same total area is used but the resistors have a 4:1 aspect ratio?

c) Size the resistors if the INL_{kmax} yield of this part is to be 99%.

Problem 6 The amplifier shown has a performance requirement that the dc gain of the feedback amplifier must be within +/- 1% of the nominal value and the output offset voltage must be less than 10 mV. Assume the amplifier is fabricated in a process with $A_\rho = 5\Omega \bullet \mu$ and $\rho_{NOM} = 30\Omega / sq$, $\mu_n C_{OX}$=250μA/v^2, $\mu_p C_{OX} = \mu_n C_{OX}$ /3, V_{TNO}=0.4V, V_{TPO}= - 0.4V, $A_{VTON} = A_{VTOP}$ = 20mV·μ , $A_\mu = A_{COX}$ = .01 $\mu^{\frac{3}{2}}$, $A_W = A_L$=0.

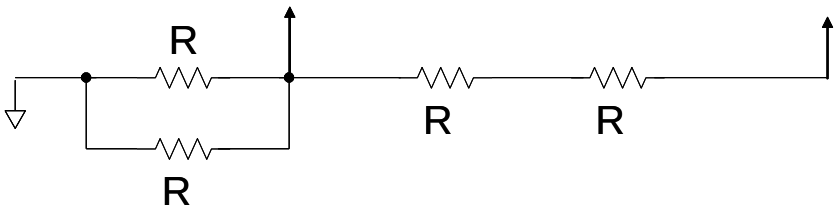


a) Determine the yield if the resistors are square with total resistor area of 100μ^2 and the operational amplifier is ideal.

b) Determine the yield if the resistors are ideal but the input stage of the operational amplifier has a source-coupled n-channel pair with W/L = 60μ/1μ and a current-mirror p-channel load with W/L=30μ /10μ.

c) Determine the yield if both nonideal effects are present

d) Assume the op amp is ideal. If the total resistive area remains fixed but instead of having 5 resistors in series for the feedback network, the feedback network shown below is used. How will the yield change from what was obtained in part a)?



Problem 7

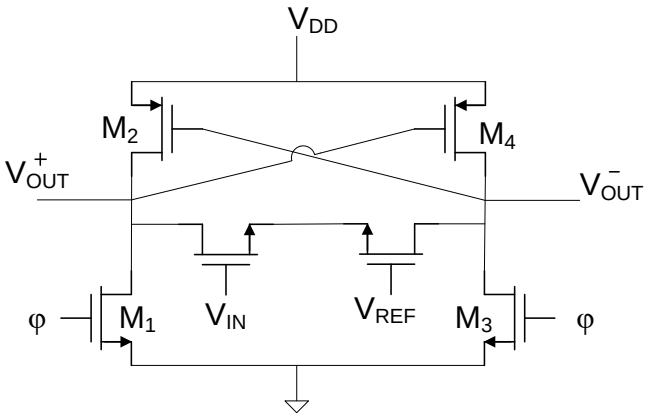
The quantization noise in a DAC is nearly uniformly distributed throughout the spectrum when near full scale sinusoids or triangle excitations are applied to the DAC. This quantization noise will be present in the DFT coefficients.

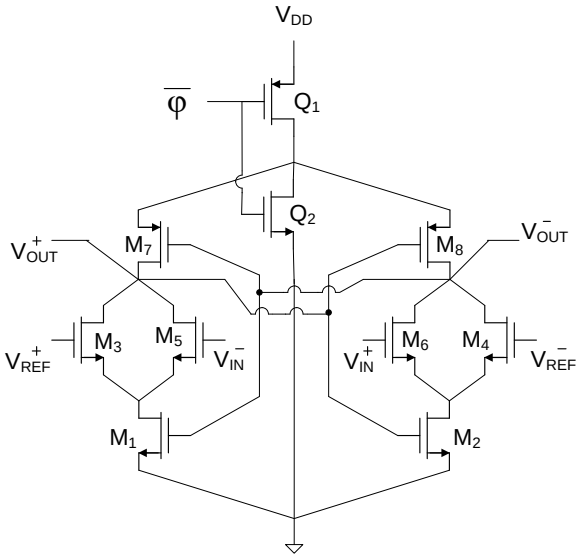
a) If all of the nonharmonic DFT coefficients are of approximately equal magnitude, determine the magnitude of these coefficients as a function of N and Np (number of periods) due to quantization noise. Assume the DAC has a single-ended output and a V_{REF} relative to ground of 1V.

b) By simulation of a 12-bit DAC, verify that the total noise in all of the DFT coefficients accurately accounts for all of the quantization noise.

Problem 8

The following two circuits, maybe new, have been proposed as dynamic comparators to compare V_{IN} with V_{REF} where ϕ is the clock that triggers the comparison. Will they function as dynamic comparators? If not, why? If so, comment on their performance.





Problem 9 A basic current-steering DAC using unary current generating elements, shown with the blocks labeled X_i, is shown below. If the switches and the op amp are ideal, any circuit can be used to generate the currents with the only requirement being that the current generating elements are matched. Several different current generating elements have been discussed in the lectures. Two of the most popular are shown below. Assume that the DAC will be used as a sub-circuit on a large ASIC with a requirement that a 10-bit DAC must be at least 99% with an $ENOB_{INL}$ of 9.5 bits Assume that everything is ideal except the statistical mismatch in the unary current generators. Which is most practical depends dominantly on the statistical matching characteristics of the components used to build the unary current generators (as determined by the Pelgrom parameters) in a given process.

a) Considering only the cost associated with the area required to realize the unary current generators, which of the two current generators will provide the lowest cost to build the 10-bit DAC in a TSMC 180nm process..
b) What is the area required to achieve the 99% yield with the two alternatives.
c) What is the ratio of the cost of the lowest cost generator to that of the highest cost generator.